REMARKS

Claims 1-9, 11-20, 22-31, and 33 were previously pending in this application. By this amendment, claims 1, 12, and 23 have been amended. New claims 34-36 have been added. As a result claims 1-9, 11-20, 22-31 and 33-36 are pending for examination with claims 1, 12, and 23 being independent claims. No new matter has been added.

Examiner Interview

Applicant wishes to thank Examiner Maskulinski for the courtesies extended in the interviews conducted on December 4, 2002, December 11, 2002, and January 8, 2003. Applicant's representative contacted Examiner Maskulinski to discuss the Advisory Action mailed November 13, 2002 (hereinafter, the "Advisory Action"). The Advisory Action maintained art rejections previously set forth in the Final Office Action mailed August 1, 2002 (hereinafter, the "Office Action"). A summary of the substance of the interviews is provided below.

In the interviews, patentability of the independent claims were discussed with respect to a §103 rejection of each of the independent claims. In the Office Action, claims 1-5, 12-16, and 23-27 were rejected as being unpatentable over U.S. Patent No. 5,289,587 to Razban (hereinafter "Razban") in further in view of U.S. Patent No. 5,862,371 to Levine et al. (hereinafter "Levine"). The Examiner, in paragraph 3 of the Office Action has taken the position that it would have been obvious at the time of the invention to include the implementation of components of a microcomputer on the same integrated circuit of Levine into the system of Razban, as Levine teaches an internal performance monitor that is located on-chip.

As discussed, Applicant's representative pointed out that there is no motivation to combine the Levine and Razban references as suggested in the prior Office Action, as one skilled in the art reading Razban would not look to Levine for improvements to the external debugging system of Razban, because Razban teaches away from using on-chip components to monitor system bus traffic, and it is an object of Razban to eliminate conventional bus monitoring as taught by Levine (please see abstract of Razban). In particular, Levine teaches an improvement of a conventional bus monitoring system (please see abstract of Levine, and col. 2, lines 33-51) that depends on monitoring the system bus. Although the Examiner considered

these arguments, he believed that the Razban and Levine references could be combined, and believed that the independent claims did not sufficiently distinguish over the combination. Applicant maintained that this combination was improper, and that the claims as presented did distinguish over the references, either alone or in combination.

Also in the interview, Applicant's representative indicated that Razban did not transmit a value of a program counter on-chip and therefore was unable to perform on-chip debug functions relating to the program counter. Further, Applicant's representative pointed out that because, according to various aspects of the present invention, program counter information was shadowed on-chip, systems (such as external debugging systems) may access such program counter information without affecting processor operations. Examiner Maskulinski indicated that the independent claims would sufficiently distinguish over the combination of Razban and Levine if the claims were to recite that the value of the program counter was being transmitted on-chip in real time. Without acceding to the appropriateness of this rejection of the claims over this combination of references or that the combination set forth is proper, Applicant agreed to amend the independent claims to recite that program counter information was being transferred to the debug circuit in real time. A more detailed discussion of the claim rejections and amended claims follows.

Rejections Under 35 U.S.C. §103

The Advisory Action rejected claims 1-5, 12-16, and 23-27 under 35 U.S.C. §103(a) as being unpatentable over Razban, (U.S. Patent No. 5,289,587, hereinafter "Razban") and further in view of Levine et al., (U.S. Patent No. 5,862,371, hereinafter "Levine"). As discussed above, the Examiner has taken the position that it would have been obvious at the time of the invention to include components of a microcomputer on the same integrated circuit of Levine into the system of Razban, as Levine teaches an internal performance monitor that is located on-chip. Applicant respectfully traverses this rejection.

As discussed in the Applicant's previous response, Razban is directed to a method for providing a microprocessor's program counter value external to a device on a dedicated bus so that an external in-circuit emulator system can generate a list of executed instruction addresses (col. 1, lines 17-21). In-circuit emulators (or ICE systems, as are known in the art) are a

combination of external software and hardware used to design and troubleshoot software programs executing on a target microprocessor or controller. Razban provides a virtual program counter value to an external ICE system via a dedicated external bus 30 (col. 4, lines 35-41, col. 4, lines 66 through col. 5, line 4). Razban eliminates the conventional requirement of monitoring system bus traffic and attempting to extract and reconstruct the instruction execution sequence (Abstract, col. 2, lines 45-57).

Levine is directed to a method and system for instruction trace reconstruction utilizing performance monitor outputs and bus monitoring (Abstract). One well-known technique for reconstructing an instruction trace includes monitoring bus traffic to determine instruction addresses, data addresses and data during the trace, if the initial architectural state of the system is known (Abstract, col. 3, lines 34-38). The difficulty in reconstructing an instruction trace from monitored bus traffic can be decreased substantially if more definitive information regarding the actual instruction sequence can be obtained (Abstract, col. 3, lines 38-41. To this end, an internal performance monitor within the processor system is utilized to generate an output each processor clock cycle which is indicative of the exact number of instructions which were executed during that clock cycle, an indication of whether or not a branch instruction was taken or not taken, an offset for each interrupt vector which has been taken, the number of data cache misses, the number of instruction cache misses, the number of store conditional instructions which were executed and the number of store conditional instructions which failed (Abstract, col. 3, lines 41-51). According to Levine, this information, in combination with monitored bus traffic may be utilized to efficiently and accurately reconstruct an instruction trace without adversely affecting performance of the system under test (Abstract, col. 3, lines 51-55). Without the necessity of actually outputting each instruction which has been executed in a manner utilized in the prior art, the performance monitor of Levine, by outputting the above parameters, can be utilized to efficiently and accurately reconstruct an instruction trace with minimal disruption of the system under test (col. 3, lines 52-55, col. 9, lines 7-13).

Applicant respectfully disagrees with the Examiner with regard to motivation for combining the references in the manner suggested. More particularly, there is no teaching or suggestion to combine the Razban and Levine references. The Examiner alleges, in paragraph three (on page 2 of the Office Action) that it "would have been obvious to one of ordinary skill at

the time of the invention to include the implementation of components of the microcomputer on the same integrated circuit of Levine into the system of Razban," because Levine implements an internal performance monitor on-chip as discussed on page 2 of the Office Action. Applicant respectfully disagrees with this assertion. As discussed above, one skilled in the art would not be motivated to combine the Razban and Levine references as Razban teaches away from using components to monitor system bus traffic such as those taught by Levine because it is an object of Razban to eliminate this conventional bus monitoring requirement (please see Abstract of Razban).

Because the Razban reference teaches away from using bus monitoring as taught by Levine, the combination of Levine and Razban is improper and the rejection should be withdrawn. A prior art reference may be considered to teach away when "a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." See *In re Gurley*, 27 F.3d 551, 553, 31 USPQ 2d 1130, 1131 (Fed. Cir. 1994). "A reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." Id. Here, the object of Razban is to eliminate bus monitoring as taught by Levine, and therefore, one skilled in the art would not be led to combine these references.

In view of the foregoing, the only motivation for combining the reference is found in the Applicant's application and this is improper. Because the motivation stated by the Examiner is not supported by evidence of the alleged motivation in the references, the rejection is improper and must be withdrawn. See *In re Dembiczak 175 F.3d 994, 50 U.S.P.Q.2d (BNA) 1614 (Fed. Cir. 1999)*. ("Combining prior art references without *evidence* of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight." [emphasis added])

Further, even if the references were combined as suggested by the Examiner, claim 1 distinguishes over the combination. In particular, the references, when combined, do not teach or suggest "a communication link coupling the processor and the debug circuit, wherein the

processor is configured to transmit, to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the processor," as recited in claim 1. As discussed above and agreed to by the Examiner, Razban does not transmit the program counter to the debug circuit in real time, Razban only transmits the program counter off-chip to an external system, and this system generally receives information at a much slower rate than an on-chip system. Levine does not supply the missing limitation, as Levine merely monitors output instructions and their addresses as they are moved into the processor on the bus, the number of instructions executed during each clock cycle, the number of interrupts, and whether branch conditional instructions were taken or not taken (Abstract, col. 8, line 59 through col. 9, line 13). Levine clearly indicates that the above parameters (and only the above parameters) are needed to reconstruct instruction trace; Levine does not transmit a value of a program counter. Therefore, even if combined, claim 1 distinguishes over the combination. Thus, the combination is first improper, and second, the combination does not render obvious claim 1. Therefore, the rejection should be withdrawn. Claims 2-9, 11, and 34 depend from claim 1 and are allowable for at least the same reasons.

Independent Claim 12

Independent claim 12 recites a microprocessor comprising at least one processor, a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the processor and debug circuit, and means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the processor.

As discussed above with reference to claim 1, the combination of Razban and Levine is improper. Further, even if the references are combined in the manner suggested, claim 12 patentably distinguishes over the combination. More particularly, neither reference teaches or suggests "means for transmitting, to the debug circuit in real time, a program counter value indicating the program counter of the processor," as recited in claim 12. As discussed above with reference to claim 1, neither Razban nor Levine teaches or suggests transmitting a program counter value in real time to a debug circuit. Therefore, the combination of cited

references is first, improper, and second, claim 12 distinguishes over the combination. Therefore, the rejection of claim 12 should be withdrawn. Claims 13-20, 22, and 35 depend from claim 12 and are allowable for at least the same reasons.

Independent Claim 23

Independent claim 23 recites a method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.

As discussed above with reference to claim 1, the combination of Razban and Levine is improper. Further, even if the references are combined in the manner suggested, independent claim 23 patentably distinguishes over the combination. More particularly, neither reference teaches or suggests "transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor," as recited in claim 23. As discussed above with reference to claim 1, neither Razban nor Levine teaches or suggests transmitting a program counter value in real time to a debug circuit. Therefore, the combination of references is first, improper, and second, claim 23 distinguishes over the combination. Therefore, the rejection of claim 23 should be withdrawn. Claims 24-33, and 36 depend from claim 23 and are allowable for at least the same reasons.

Added Claims

Claims 34-36 were added to further define Applicant's contribution to the art. These claims are allowable for at least the same reasons as the claims from which they depend.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

Respectfully submitted,

David Alan Edwards, Applicant

By: _____

Edward J. Russavage, Reg. No. 43,069
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Telephone: (617) 720-3500

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MARKED-UP CLAIMS

1. (Amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the processor.

12. (Amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and

means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the processor.

23. (Amended) A method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of:

transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.